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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/424,544	11/24/1999	MASUMITSU INO	SON-1582/SUG	8128

7590 06/17/2002

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ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 06/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/424,544	Applicant(s) INO ET AL.	
	Examiner Jeff Piziali	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Petition

1. Applicants' petition filed on February 27, 2002 (paper no. 9) is considered a request for reconsideration, and is deemed persuasive. The restriction requirement mailed on August 17, 2001 (paper no. 5) is hereby withdrawn. Claims 1-39 are now pending in the present application.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 27, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-12 and 17-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. (US 4,825,203).

Regarding claim 1, Takeda et al. discloses a liquid crystal display [Fig. 2, 11] comprising: a display portion in which a plurality of pixels [Fig. 2, 11-c] are two-dimensionally arranged at intersecting points of gate lines [Fig. 2, 11-a] as many as a plurality of rows and signal lines [Fig. 2, 11-b] as many as a plurality of columns which are wired in a matrix shape; and a plurality of driver circuits [Figs. 1(A) & 2, 13 & q_1-q_N] for applying a signal potential to each pixel in the display portion through the signal lines of the plurality of columns, characterized in that when the plurality of driver circuits are arranged in order while the numbers of output terminals of the driver circuits are set to a same number [i.e. 3] so as to have a correspondence relation with each of the signal lines of the plurality of columns, if a fraction [i.e. 3/1] occurs in the signal lines of the plurality of signal lines of the plurality of columns, the number of output terminals of one of the plurality of driver circuits is set to the fraction (see Column 2, Line 56 - Column 4, Line 68).

Regarding claim 2, Takeda et al. discloses the driver circuits are driver ICs arranged an outside of a transparent insulating substrate on which the display portion is formed (see Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Regarding claim 3, Takeda et al. discloses a liquid crystal display [Fig. 2, 11] comprising a display portion in which a plurality of pixels [Fig. 2, 11-c] are two-dimensionally arranged at intersecting points of gate lines [Fig. 2, 11-a] as many as a plurality of rows and signal lines [Fig. 2, 11-b] as many as a plurality of columns which are wired in a matrix shape; and a plurality of driver circuits [Figs. 1(A) & 2, 13 & q_1-q_n] for applying a signal potential to each pixel in the display portion through the signal lines of the plurality of columns (see Column 2, Line 56 - Column 3, Line 27), characterized in that the number of output terminals [i.e. 3] of each of the plurality of driver circuits is set to a measure of the total number of signal lines [i.e. N] of the plurality of columns (see Column 4, Lines 22-46).

Regarding claim 4, this claim is rejected by the reasoning applied in the above rejection of claim 1.

Regarding claim 5, Takeda et al. discloses that the number of output terminals of each of the plurality of the driver circuits is set to a power of 2 (i.e. $2^n = 3$).

Regarding claim 6, this claim is rejected by the reasoning applied in the above rejection of claim 2.

Regarding claim 7, Takeda et al. discloses a memory circuit [Fig. 1(A), 31] for temporarily storing data [Fig. 1(A), D] to be written into the driver circuits; and a control circuit [Fig. 2, 15] for controlling the driver circuits so as to simultaneously write different data from the memory circuit (see Column 3, Lines 8-27 & Column 4, Lines 22-68).

Regarding claim 8, Takeda et al. discloses that when a size of a frame portion [Fig. 1(A), q_N] adjacent to the display portion is specified, the number [i.e. n = 3] of output terminals of each of the driver circuits is determined on the basis of the specified frame size by the number of lines which ca be wired into a wiring region of the frame portion (see Column 4, Lines 22-68).

Regarding claim 9, Takeda et al. discloses the total number of signal lines of the plurality of columns which is decided by a display system is set to N [Fig. 1(A), Q], the number of the driver circuits is set to N/n [Fig. 1(A), q] (see Column 4, Lines 22-68).

Regarding claim 10, Takeda et al. discloses time-divisional switches [Fig. 1(A), 32] for time-divisionally sending a signal potential [Fig. 1(A), V_R, V_G & V_B] which is outputted from each of the plurality of driver circuits to the signal lines of the plurality of columns (see Column 4, Lines 22-46).

Regarding claim 11, Takeda et al. discloses a leading waveform and a trailing waveform of a signal output waveform [Fig. 1(B), C_R, C_G & C_B] of each of the plurality of driver circuits are symmetrical with respect to a time base (see Column 4, Lines 47-68).

Regarding claim 12, Takeda et al. discloses a time-dividing number of the time-divisional switches is equal to three [see Fig. 1(A), 32].

Regarding claim 17, Takeda et al. discloses the plurality of driver circuits generate a signal potential so as to correct shift amounts of curves of voltage-transmittance characteristics of red, green and blue [see Fig. 1(A), V_R, V_G & V_B], by driving the time-divisional switches (see Column 4, Lines 22-46).

Regarding claim 18, Takeda et al. discloses a 1H (H denoting a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by the time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red [see Fig. 4(B); Row i+2 & Columns j, j+1 and j+2].

Regarding claim 19, Takeda et al. discloses a dot inversion driving, the signal line which is selected first by the time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue [see Fig. 5(B); Row i & Columns j, j+1 and j+2].

Regarding claim 20, Takeda et al. discloses time-division of the time-divisional switches distribute signals to red, green and blue constituting one pixel [see Figs. 4(A-B); Column 5, Lines 16-58].

Regarding claim 21, Takeda et al. discloses a surplus connecting region [Fig. 2; 12, 13, & 15] that does not contribute to the display portion [Fig. 2, 11] does not occur on the display (see Column 2, Line 56 - Column 3, Line 27).

Regarding claim 22, Takeda et al. discloses a driver circuit of the plurality of driver circuits is separate and distinct from another driver circuit of the plurality of driver circuits (see Fig. 1(A)).

Regarding claim 23, this claim is rejected by the reasoning applied in the above rejection of claim 21.

Regarding claim 24, this claim is rejected by the reasoning applied in the above rejection of claim 22.

Regarding claim 25, Takeda et al. discloses a liquid crystal display comprising: a display portion [Fig. 2, 11], the display portion having a plurality of gate lines [Fig. 2, 11-a], a plurality of signal lines [Fig. 2, 11-b] and a plurality of pixels [Fig. 2, 11-c], a pixel of the plurality of

pixels being located at an intersection of a gate line of the plurality of gate lines and a signal line of the plurality of signal lines; and a plurality of driver circuits [Figs. 1(A) & 2, 13 & q_1-q_N], a driver circuit of the plurality of driver circuits being separate and distinct from another driver circuit of the plurality of driver circuits, each driver circuit of the plurality of driver circuits having a plurality of output terminals, the plurality of output terminals providing a plurality of signal potentials to a group of signal lines of the plurality of signal lines, the group of signal lines being less than all of the plurality of signal lines (see Column 2, Line 56 - Column 4, Line 68).

Regarding claim 26, this claim is rejected by the reasoning applied in the above rejection of claim 22.

Regarding claim 27, Takeda et al. discloses the pixels are arranged in a two-dimensional matrix shape (see Fig. 2).

Regarding claim 28, Takeda et al. discloses the pixel includes a transistor [Fig. 2, 11-d], a gate electrode [Fig. 2, 11-a] of the transistor being electrically connected to the gate line, a source/drain of the transistor [Fig. 2, 11-b] being electrically connected to the signal line (see Fig. 2; Column 2, Lines 56-68).

Regarding claim 29, Takeda et al. discloses the plurality of gate lines is a plurality of rows and the plurality of signal lines is a plurality of columns (see Fig. 2).

Regarding claim 30, Takeda et al. discloses an output terminal [Fig. 1(A), q_N] of the plurality of output terminals provides a signal potential of the plurality of signal potentials to the signal line [Fig. 1(A), Q_N] (see Column 4, Lines 22-68).

Regarding claim 31, this claim is rejected by the reasoning applied in the above rejection of claim 21.

Regarding claim 32, Takeda et al. discloses an amount [i.e. 1] of signal lines of the plurality of signal lines is connected to the driver circuit, the amount being an integer not less than 1 (see Fig. 1(A)).

Regarding claim 33, Takeda et al. discloses another amount [i.e. 1] of signal lines of the plurality of signal lines is connected to the another driver circuit, the amount being equal to the another amount, the another amount being an integer not less than 1 (see Fig. 1(A)).

Regarding claim 34, Takeda et al. discloses a remainder amount [i.e. 1] of the plurality of signal lines is less than the amount of the plurality of signal lines [i.e. 3], the remainder amount being the amount of the plurality of signal lines connected to a remainder driver circuit [Fig. 1(A), q_N] of the plurality of driver circuits, each other driver circuit of the plurality of driver circuits being connected to the amount of the plurality of signal lines (see Fig. 1(A)).

Regarding claim 35, Takeda et al. discloses another amount [i.e. 3] of the output terminals is the amount of the output terminals for the another driver circuit, the amount is equal to the another amount (see Fig. 1(A)).

Regarding claim 36, Takeda et al. discloses the aggregate number of output terminals [i.e. 3] of the plurality of driver circuits is set to a measure of the total number of the signal lines [i.e. 3] (see Fig. 1(A)).

Regarding claim 37, Takeda et al. discloses an output terminal of the plurality of output terminals is electrically connected to an input terminal of a time-divisional switch [Fig. 1(A), 32], the time-divisional switch providing a signal potential of the plurality of signal potentials to the signal line as a de-multiplexed signal potential (see Column 4, Lines 22-68).

Regarding claim 38, this claim is rejected by the reasoning applied in the above rejection of claim 20.

Regarding claim 39, Takeda et al. discloses the red signal potential is applied to a red pixel of the plurality of pixels, the green signal potential is applied to a green pixel of the plurality of pixels, and the blue signal potential is applied to a blue pixel of the plurality of pixels (see Fig. 2, Column 2, Lines 56-68).

6. Claims 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Uchino et al. (US 5,936,617).

Regarding claim 13, Uchino et al. discloses a liquid crystal display [Fig. 6, 11] comprising a display portion in which a plurality of pixels [Fig. 6, PXL] are two-dimensionally arranged at intersecting points of gate lines [Fig. 6, X] as many as a plurality of rows and signal lines [Fig. 6, Y] as many as a plurality of columns which are wired in a matrix shape; and a plurality of driver circuits [Fig. 6, 22] for applying a signal potential to each pixel in the display portion through the signal lines of the plurality of columns, characterized in that the number of output terminals of each of the plurality of driver circuits is set to a measure of the total number of signal lines of the plurality of columns (see Column 7, Lines 3-45); time-divisional switches [Fig. 6, HSW] for time-divisionally sending a signal potential [Fig. 6, Vsig out] which is outputted from each of the plurality of driver circuits to the signal lines of the plurality of columns; wherein a time-dividing number of the time-divisional switches is equal to three; and a period of time which is selected by the time-divisional switches is equal to or shorter than a third of a horizontal scanning period (see Fig. 7; Column 7, Line 46 - Column 8, Line 6).

Regarding claim 14, Uchino et al. discloses a leading time and a trailing time of each of the plurality of driver circuits are equal to or shorter than the period of time which is selected by the time-divisional switches (see Fig. 7; Column 7, Line 46 - Column 8, Line 6).

Regarding claim 15, Uchino et al. discloses a blanking period which is caused for the period of time selected by the time-divisional switches is equal to or shorter than [(a horizontal

scanning period) - (the period of time selected by the time-divisional switches x 3)] / 3 (see Fig. 7; Column 7, Line 46 - Column 8, Line 6).

Regarding claim 16, Uchino et al. discloses the plurality of driver circuits have a function to stop the operation of their output circuit for the blanking period (see Fig. 7; Column 7, Line 46 - Column 8, Line 6).

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 38 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 38 recites the limitation "said time-division switch" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Response to Arguments

10. Applicants' arguments filed February 27, 2002 (paper no. 10) have been fully considered but they are not persuasive. The applicants contend that the prior art of Takeda et al. (US 4,825,203) fails to disclose a plurality of driver circuits. The examiner respectfully disagrees. Takeda teaches a single shift register [Fig. 1(A); 31 -- which inherently consists of multiple,

separate, and distinct drivers] working in conjunction with plural driver circuits [Figs. 1(A), q_1-q_N,C_{RGB}, and 32-37] (see Column 4, Lines 22-68).

The applicants go on to argue that Takeda also fails to disclose each of the plurality of driver circuits has "a number" of output terminals. The examiner again respectfully disagrees. As is clearly illustrated in Takeda, each output of the shift register [Fig. 1(A); 31] is split into three outputs [Fig. 1(A); q_1-q_N] and then processed by three gate circuits [Fig. 1(A); 37] and three analog switches [Fig. 1(A); 32] -- at each separate stage having three (i.e. "a number") output terminals.

The applicants further contend that Takeda fails to disclose that the output terminals of each of the plurality of driver circuits is set to "a measure" of the total number of signal lines of the plurality of columns. The examiner must once more respectfully disagree. Takeda's teaches driver circuits with "a number" of output terminals (for instance, 3 -- as explained in the above paragraph) which inherently qualifies as "a measure" of the total number of signal lines [Fig. 1(A); Q_N -- for example, 3/N].

By the reasoning expressed above, the rejection of claims 1-39 is deemed proper and thereby maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
June 13, 2002

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